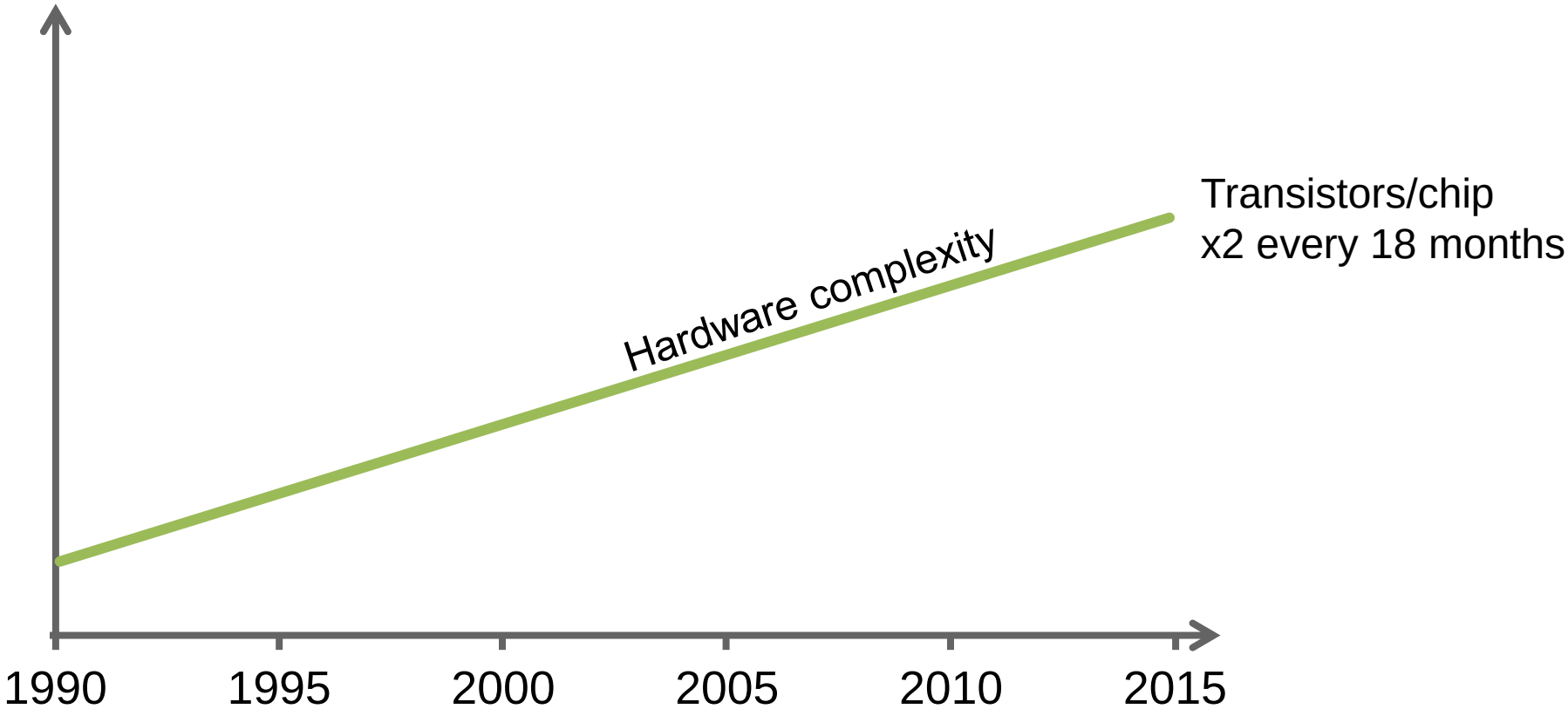
PREESM: A Dataflow-Based Rapid Prototyping Framework for Simplifying Multicore DSP Programming

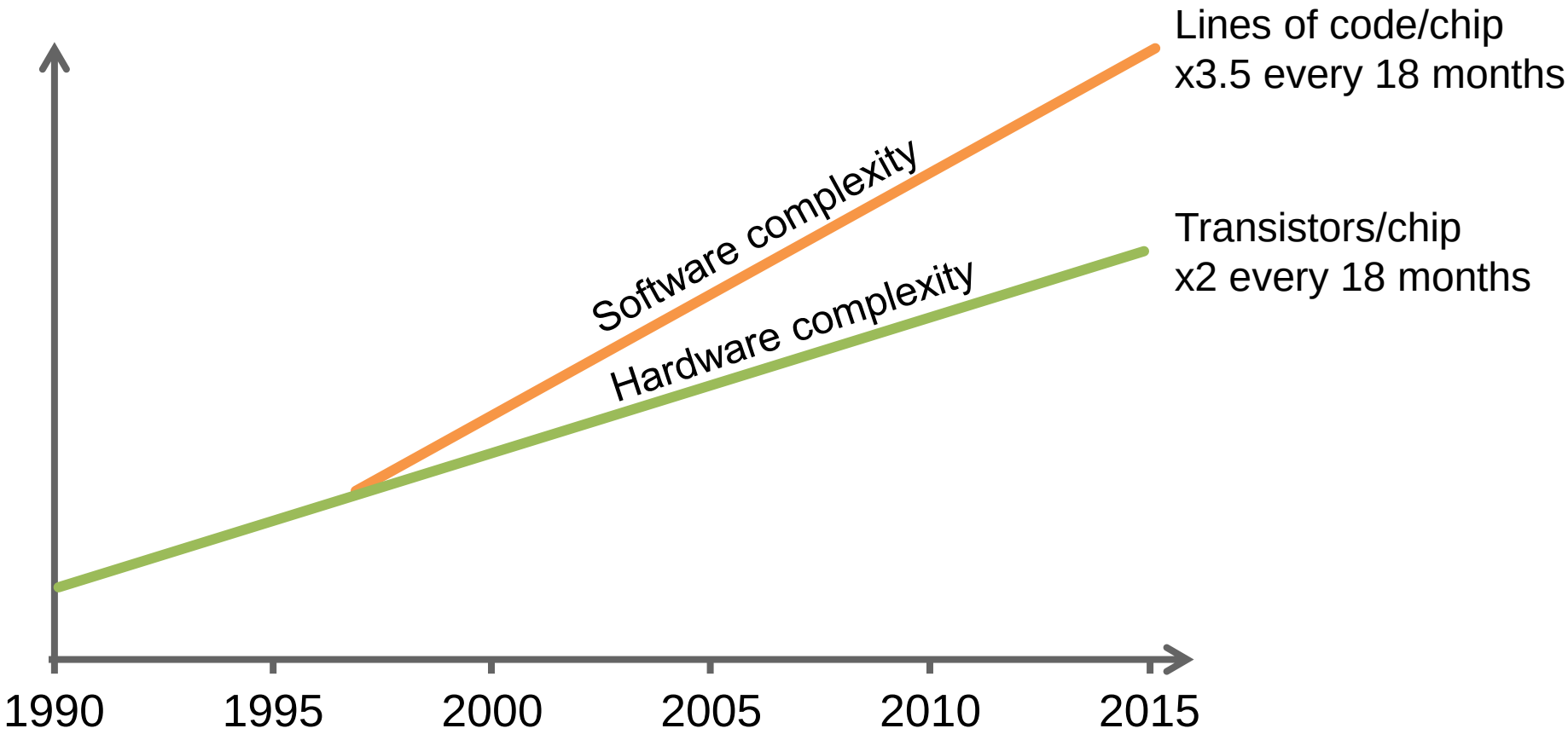
Maxime Pelcat, Karol Desnos, Julien Heulot

Clément Guy, Jean-François Nezan, Slaheddine Aridhi

EDERC 2014 Conference, Milan, September 11th



Source: “Hardware-dependent Software”, Ecker, et. al



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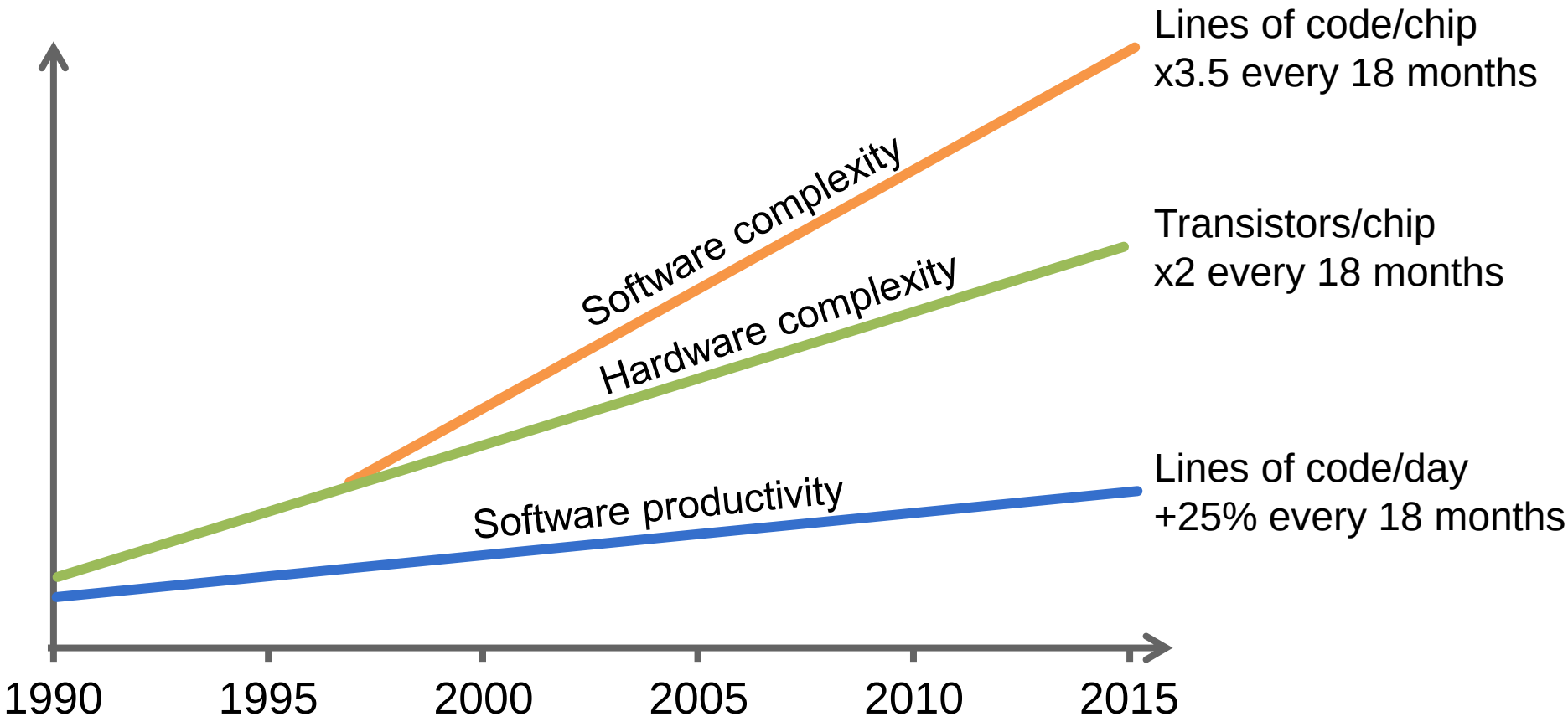

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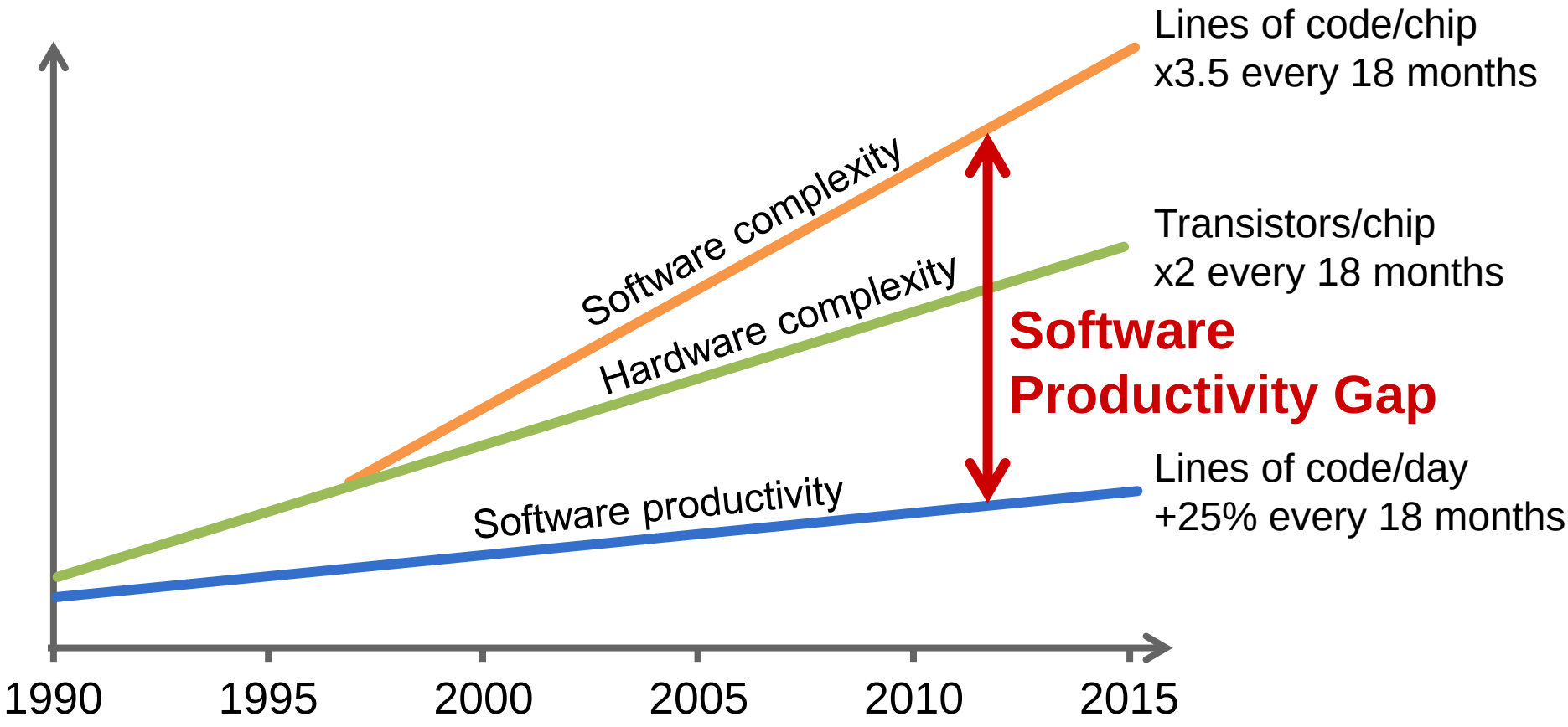

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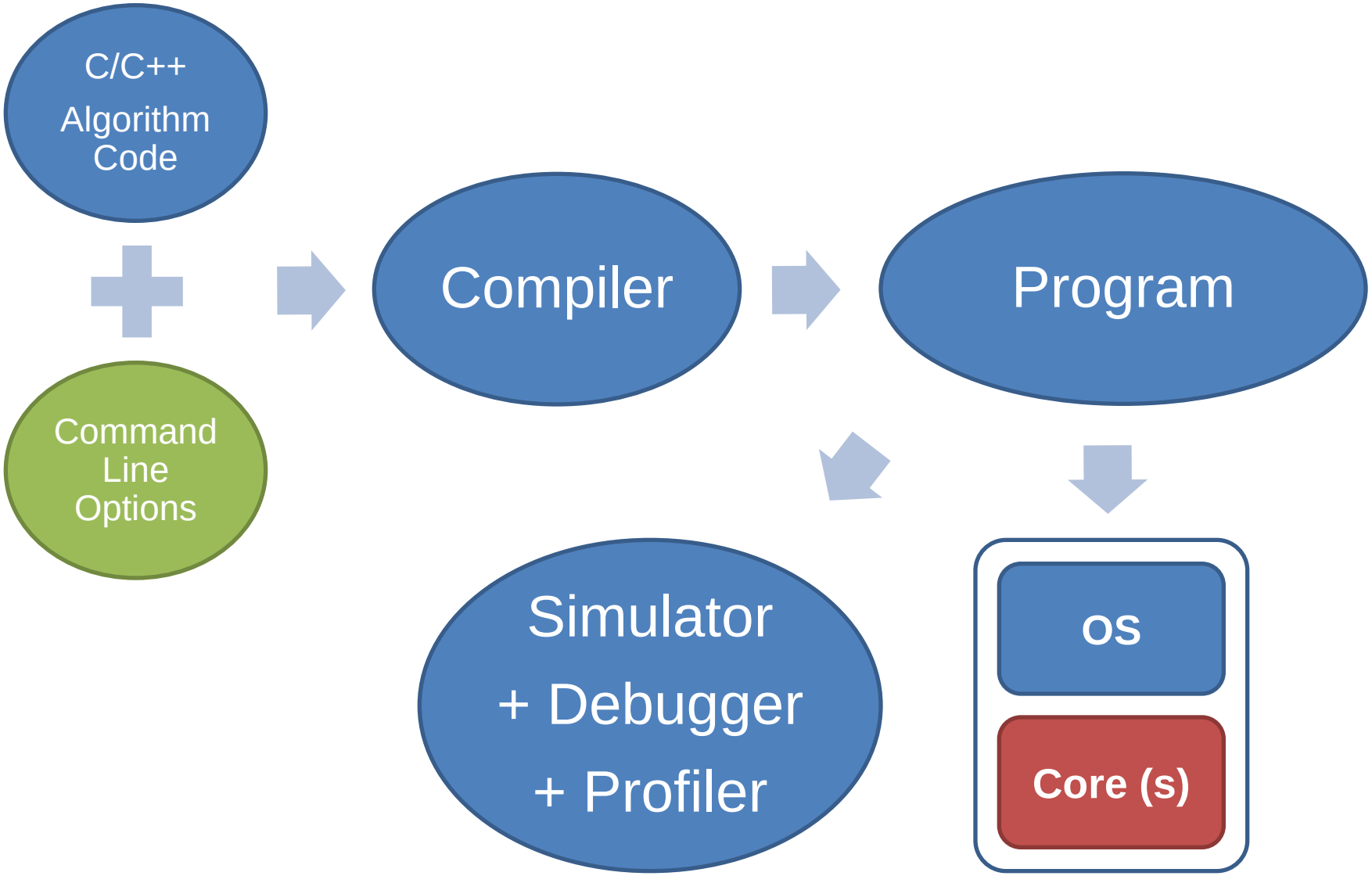
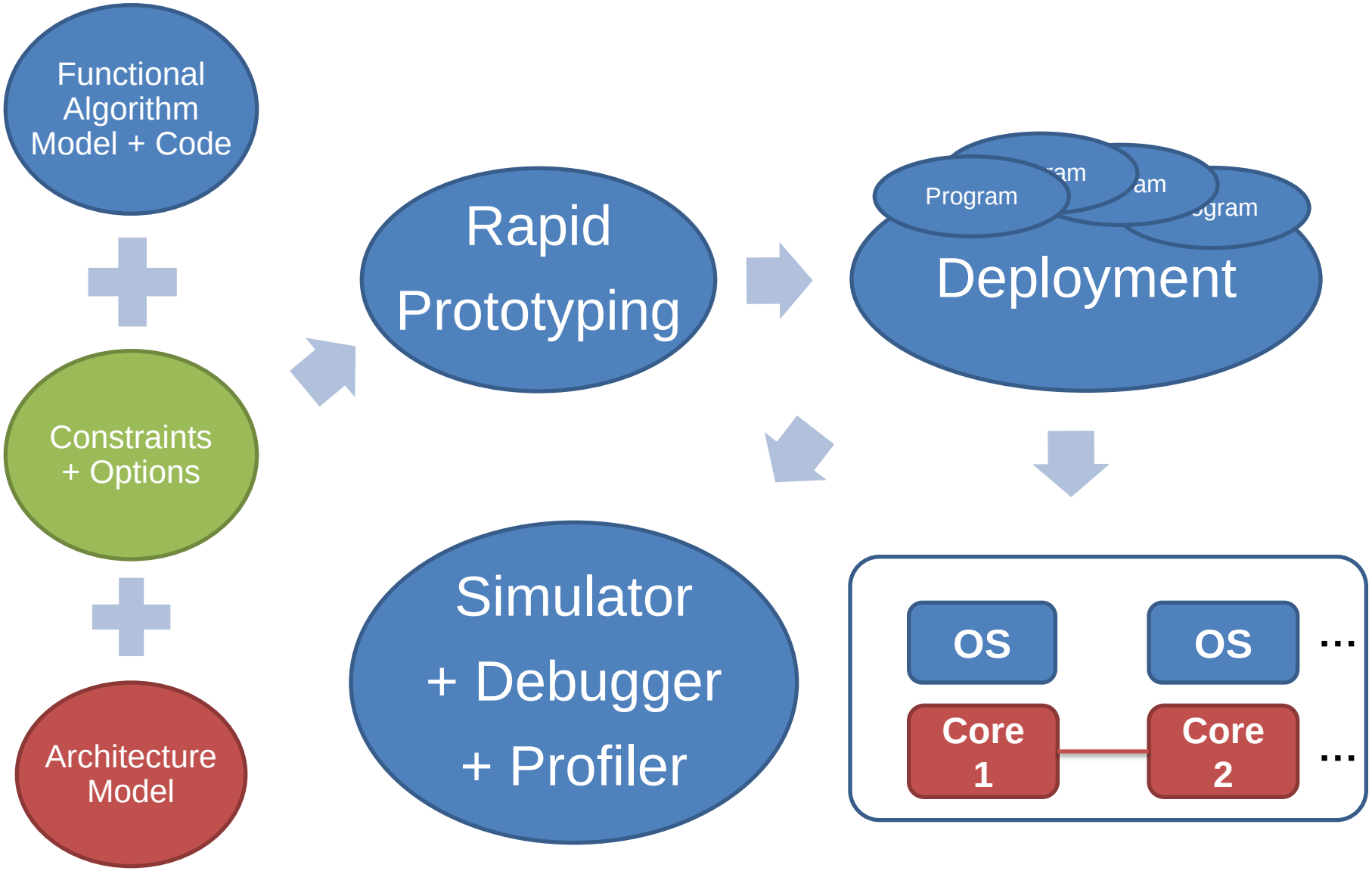
Typical Single DSP Environment



Multicore DSP Rapid Prototyping



Reduce Software Productivity Gap

- In early design phases: Metrics
- Design parallel algorithms
  - Automatic mapping and scheduling
- Predictable time and memory
  - choose the right algorithm and hardware

Reduce Software Productivity Gap

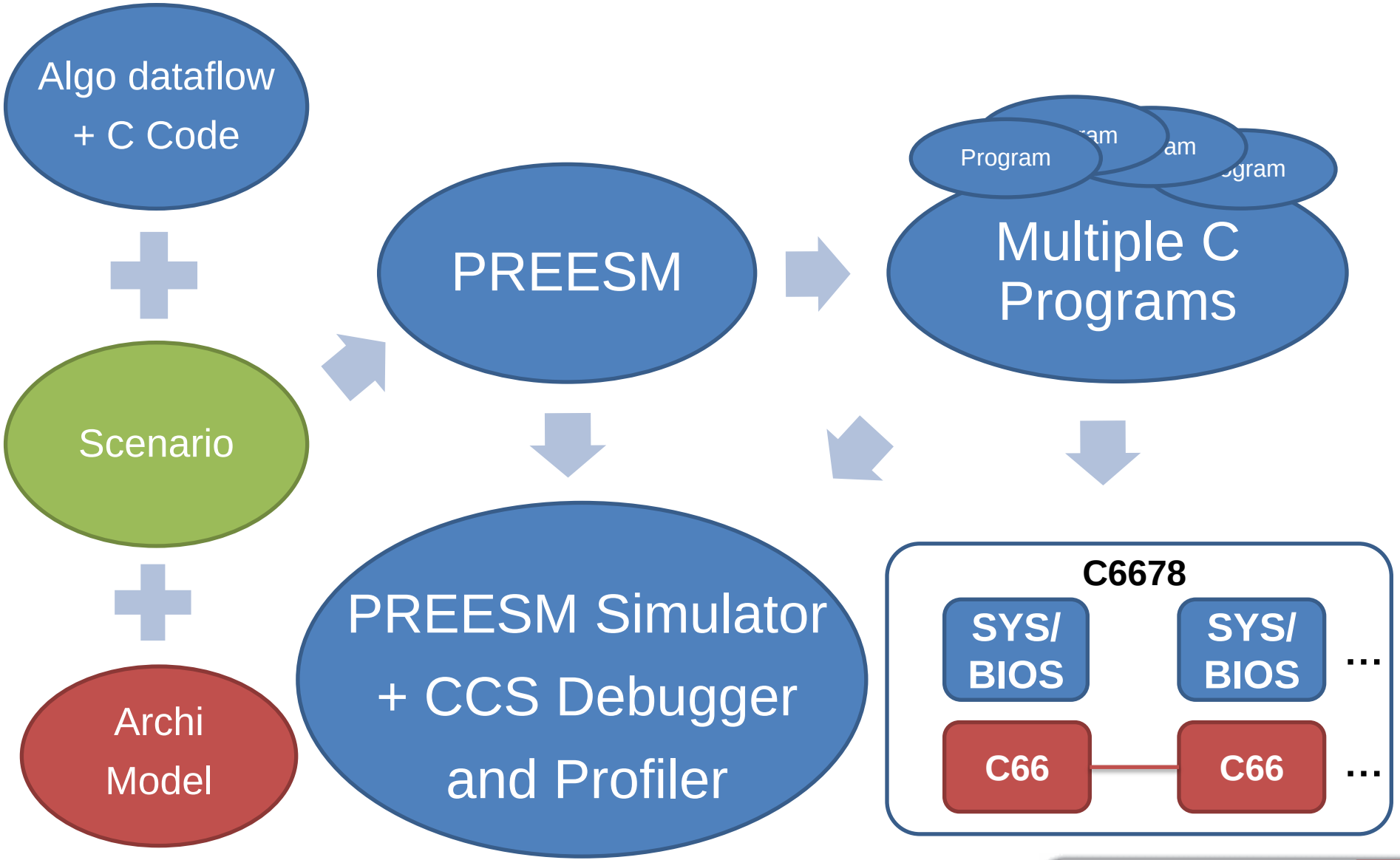
- In late design phases: Rapid Prototyping
- Automatic multi-core speedup
- Inter-core communication
- Guaranteed Deadlock-freeness

Reduce Software Productivity Gap

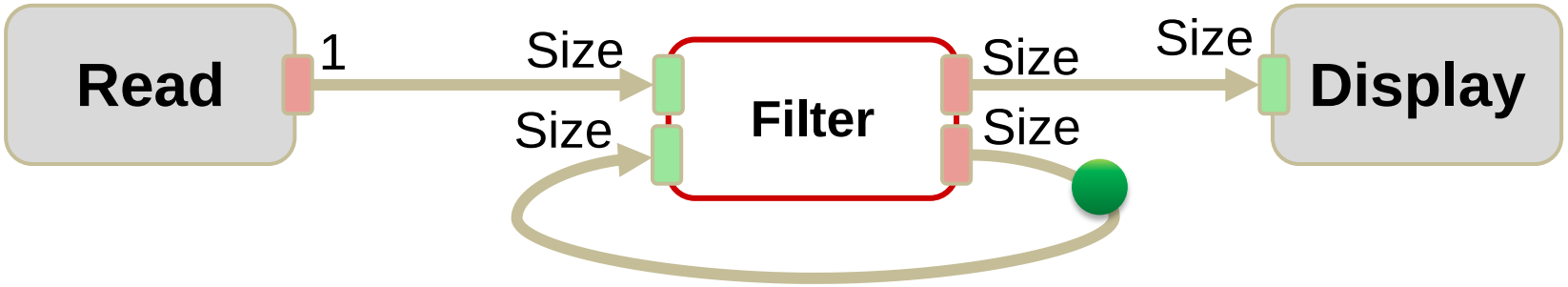
- For migration to a new hardware
- Seamless porting to a new architecture
- Legacy code reuseability
- Portable performance

→ Dataflow modelling can help

PREESM for C6678

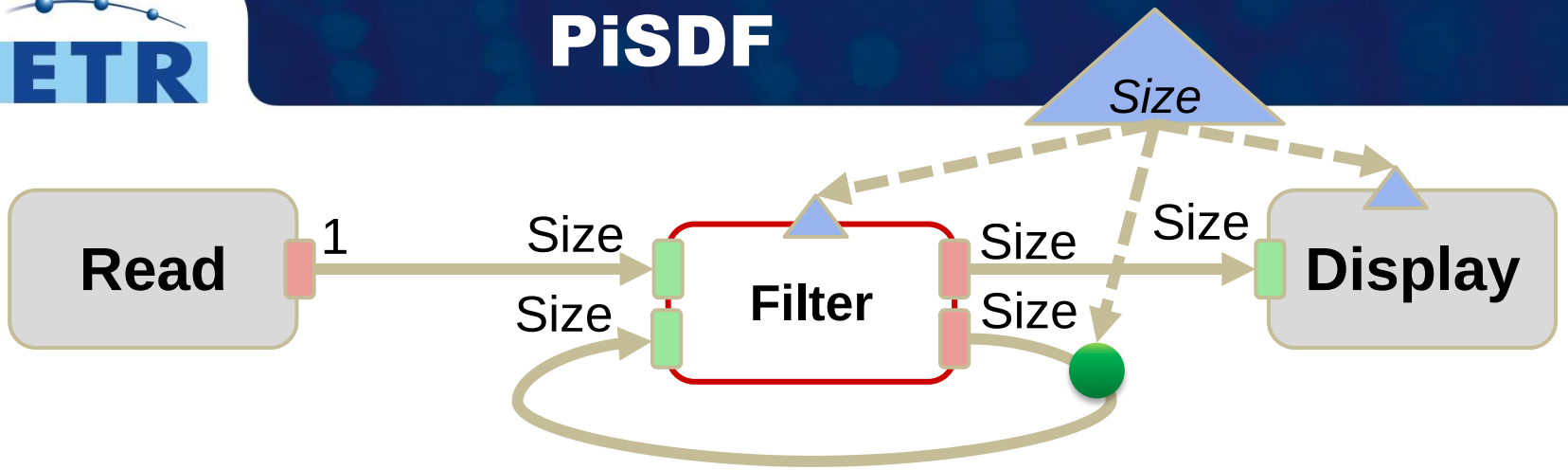


Algo dataflow: PiSDF



K. Desnos, M. Pelcat, J.-F. Nezan, S. S. Bhattacharyya, S. Aridhi “PiMM: Parameterized and Interfaced Dataflow Meta-Model for MPSoCs Runtime Reconfiguration”, SAMOS XIII

PiSDF



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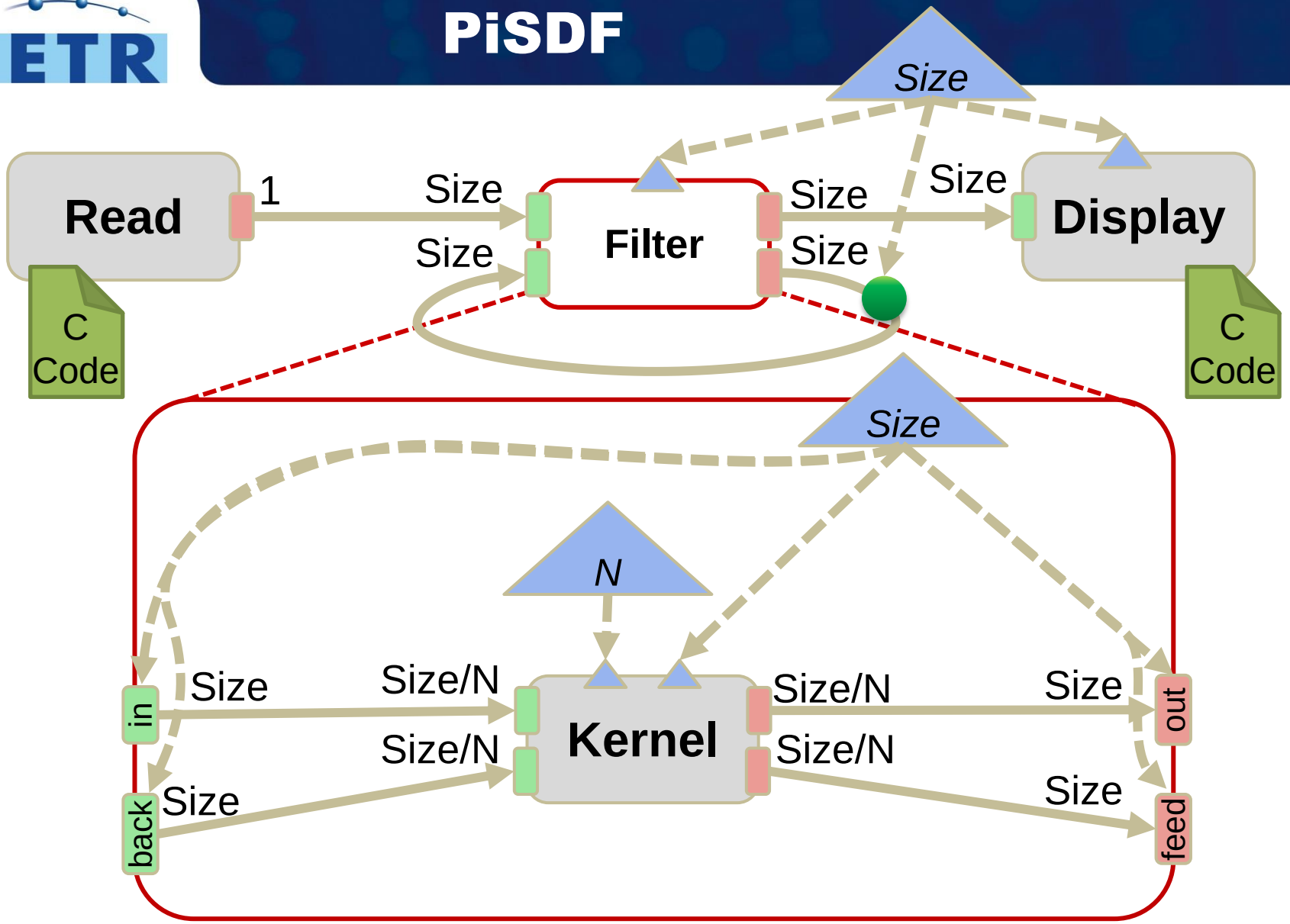
PiSDF



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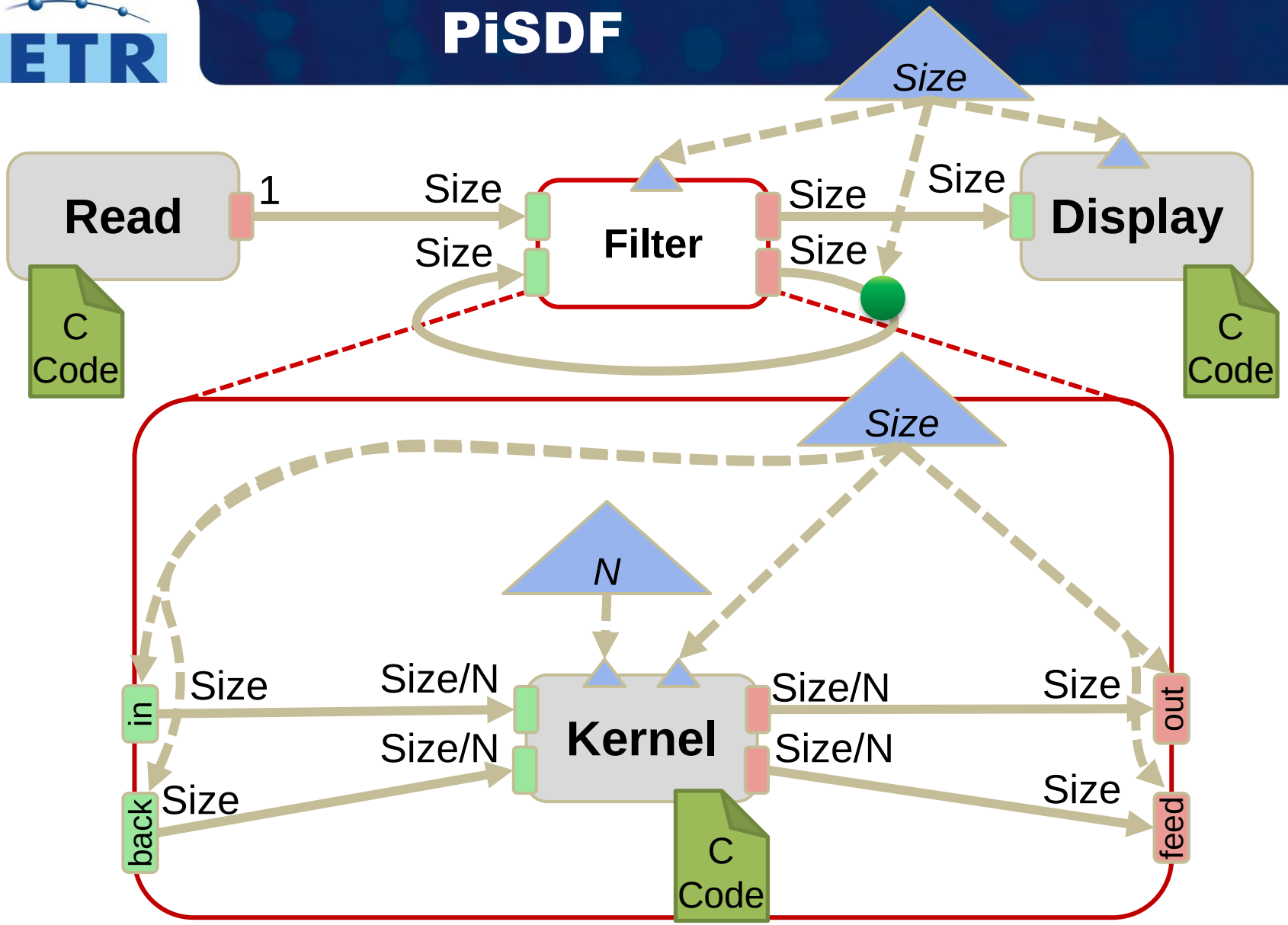
PiSDF



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Algo dataflow: PiSDF

PiSDF MoC is:

- ✓ Hierarchical & Compositional
- ✓ Statically parameterizable
- ✓ Dynamically reconfigurable

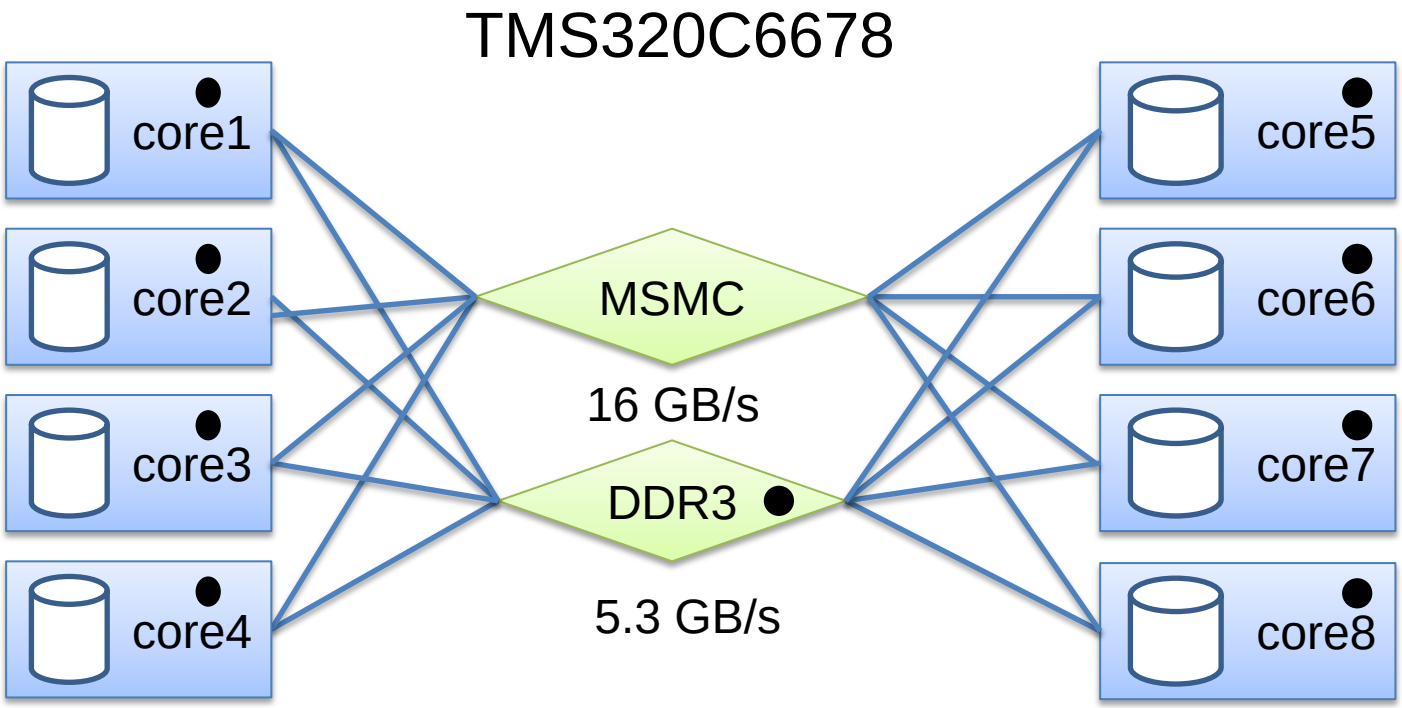
PiSDF fosters:

- Predictability
- Parallelism
- Lightweight runtime overhead
- Developer-friendliness

K. Desnos, M. Pelcat, J.-F. Nezan, S. S. Bhattacharyya, S. Aridhi “PiMM: Parameterized and Interfaced Dataflow Meta-Model for MPSoCs Runtime Reconfiguration”, SAMOS XIII

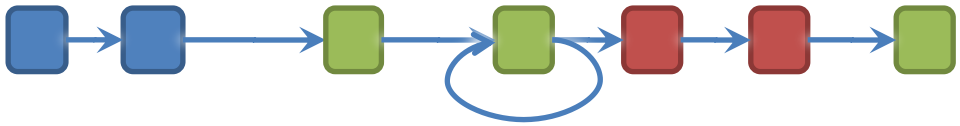
Archi: System-Level Archi. Model

- Representing contentions as TDMA



PREESM: Multicore Scheduling

- Scheduling based on latency and load balancing



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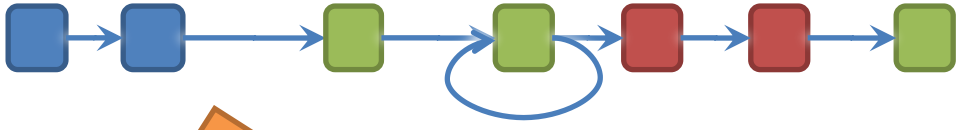

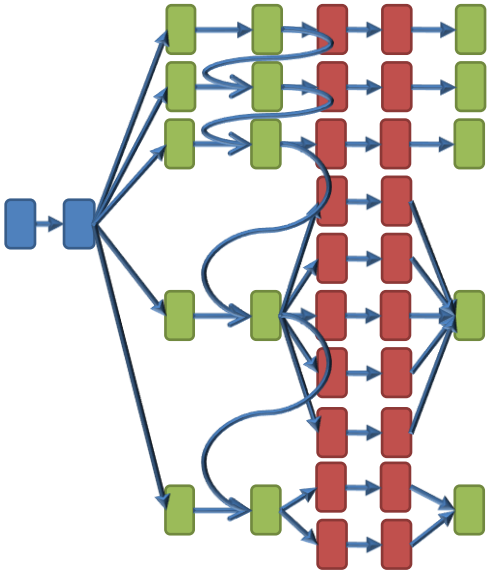

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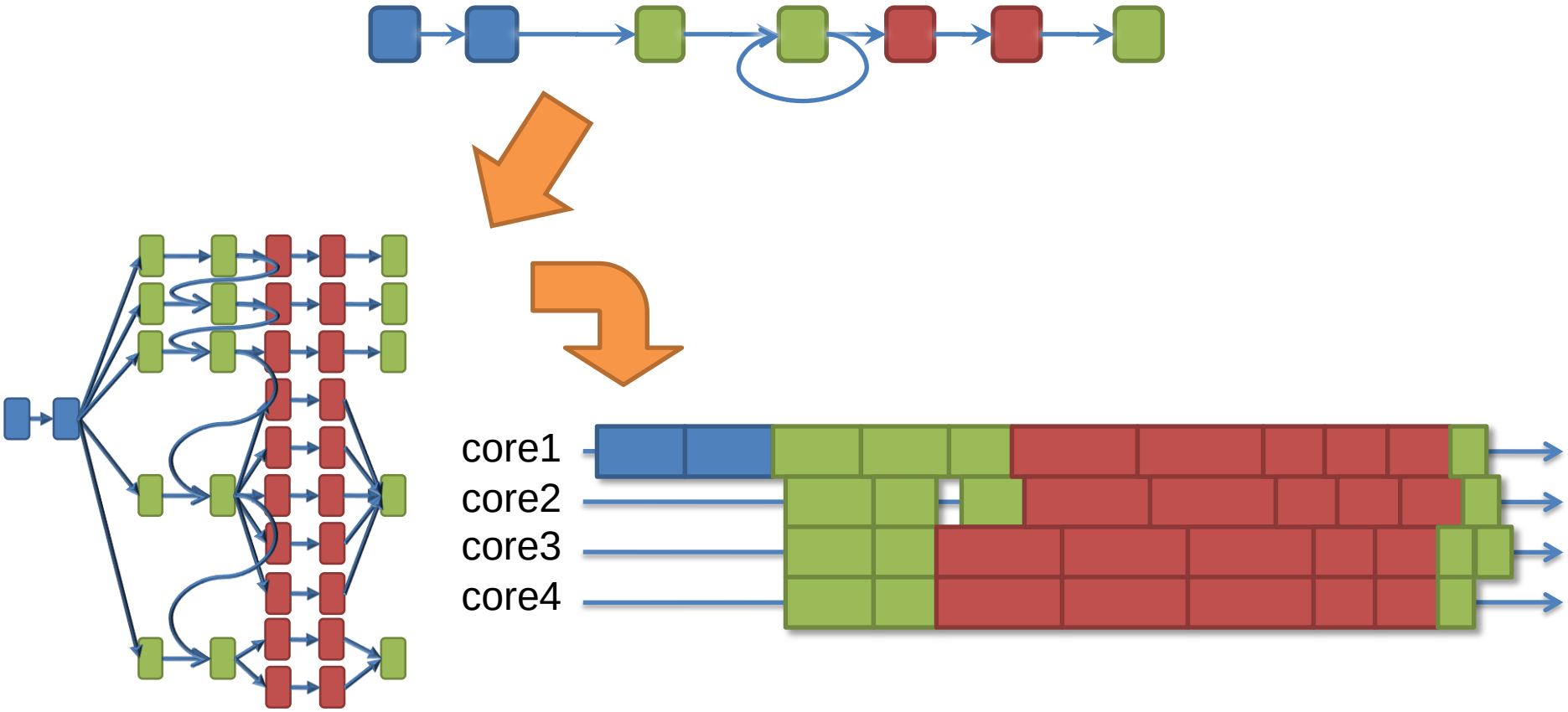
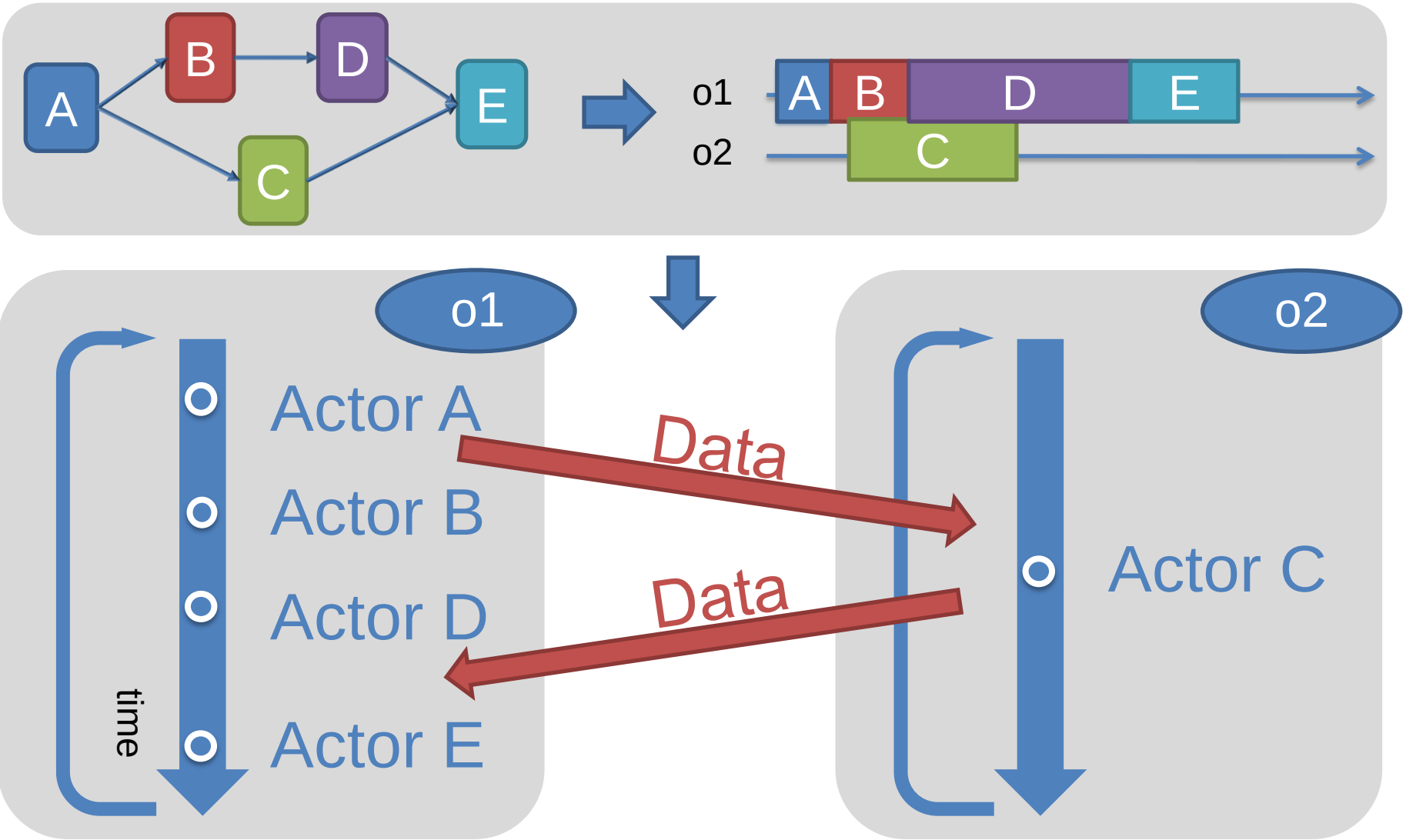


PREESM: Memory Bounds

- **Bounding the memory needs of an application graph to:**
  - Evaluate the memory requirements
  - Adjust the size of architecture memory
  - Assess the optimality of a memory allocation

PREESM: Prototype Code Generation



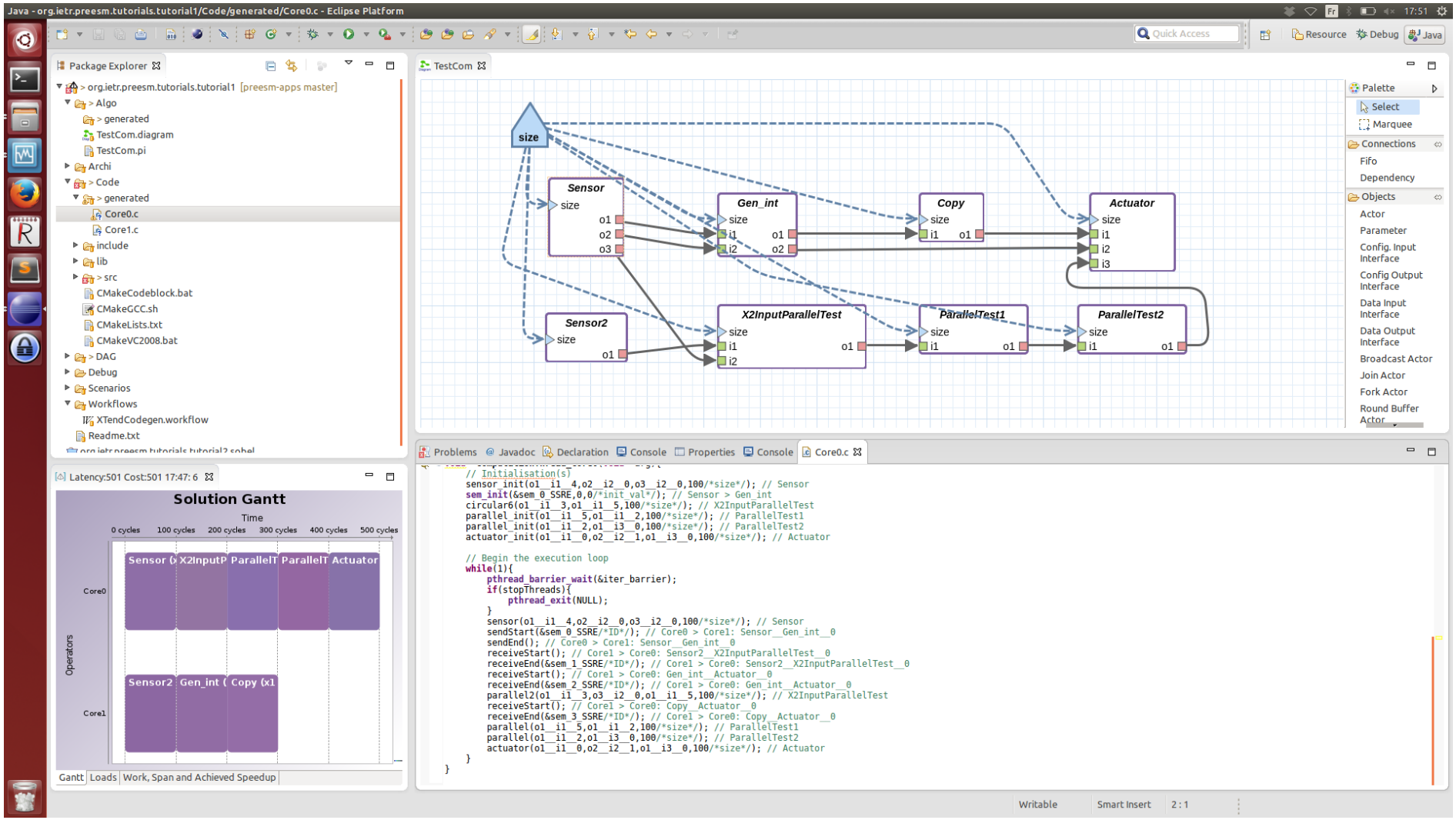
PREESM Features

- Open Source Tool
  - Available on GitHub
- Research-Oriented Tool
  - New models, optimizations, scheduling
- Eclipse-based Integrated Tool
  - Several plug-ins, metamodels
- Extended Web Tutorials
  - http://preesm.sourceforge.net/website

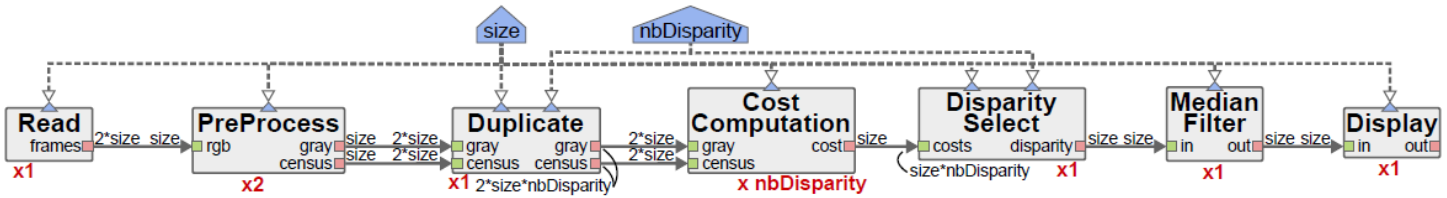
Other Tools

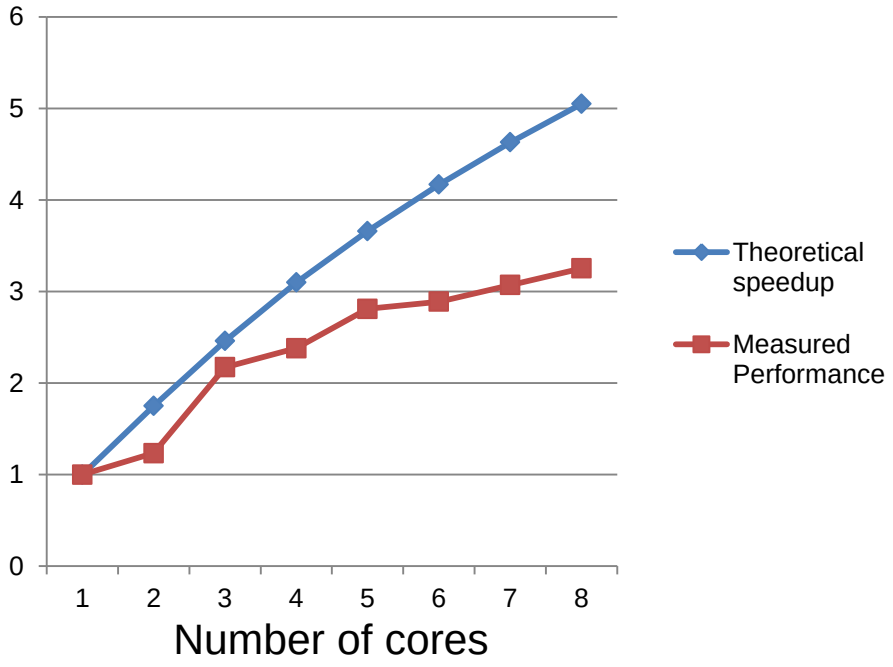
- OpenMP, OpenEM
  - Adding Rapid Prototyping
- MAPS Compiler, Polycore Polymapper, SynDEx
  - Open-source code

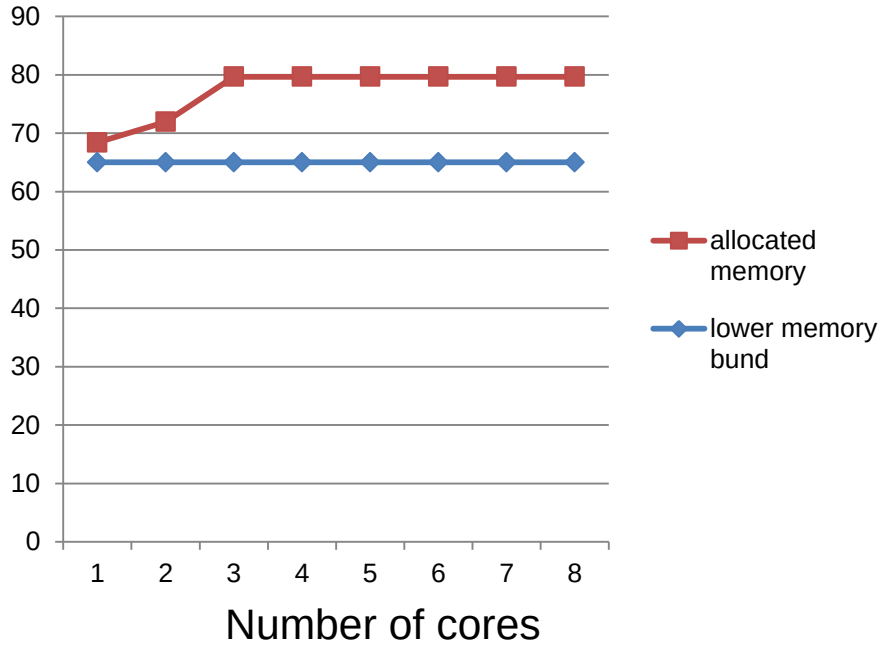
PREESM Features



Some Results on Stereo Matching







Conclusion

- Reduce Software Productivity Gap
  - Design space exploration
  - Rapid Prototyping
  - Extract coarse grain parallelism
  - Portable performance

PREESM →Dataflow modelling can help!

  - Good decisions necessitate extensive information on both computation and data flow

Thanks!

M. Pelcat, K. Desnos, J. Heulot, C. Guy, J.-F. Nezan, S. Aridhi, "**PREESM: A Dataflow-Based Rapid Prototyping Framework for Simplifying Multicore DSP Programming**" EDERC, 2014.

PREESM Tutorial – 16:00 – 17:00 - Room: Oro Plenaria

M. Pelcat, S. Aridhi, J. Piat , J.-F. Nezan, "**Physical Layer Multicore Prototyping: A Dataflow-Based Approach for LTE eNodeB**".

Springer, 2012.